



650V SuperJunction Power MOSFET

Features

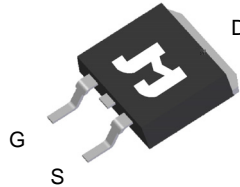
- Extremely Low Gate Charge
- Excellent Output Capacitance (C_{oss}) Profile
- Fast Switching Capability
- 100% UIS Tested, 100% R_g Tested
- Pb-free Lead Plating
- Halogen-free

Product Summary

Parameter	Value	Unit
V_{DS}	650	V
$V_{GS(th)}_{Typ}$	3.5	V
I_D (@ $V_{GS} = 10V$) ⁽¹⁾	35.0	A
$R_{DS(ON)}_{Typ}$ (@ $V_{GS} = 10V$)	98	m Ω
$E_{oss@400V}$		

- Switching Applications

TO-220-3L Top View

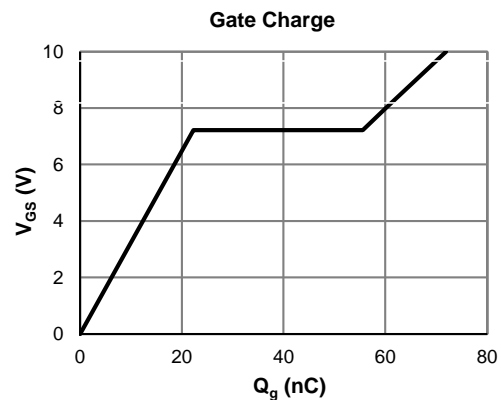
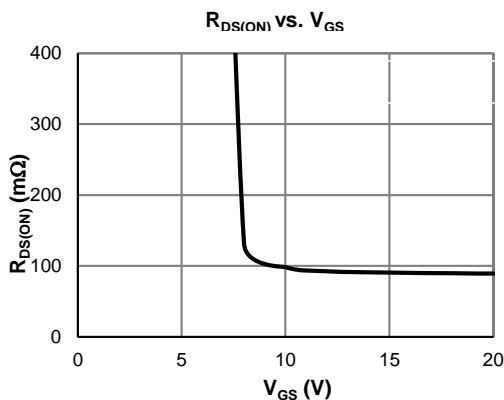


Ordering Information

Device							
JMH65R110ACFD-U							
JMH65R110AEFD-13							

Absolute Maximum Ratings (@ $T_A = 25^\circ C$ unless otherwise specified)

Parameter		Value	
Drain-to-Source Voltage		650	
Gate-to-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current ⁽¹⁾	$T_C = 25^\circ C$	35	A
	$T_C = 100^\circ C$	21	
Pulsed Drain Current ⁽²⁾	I_{DM}	137	A
Avalanche Current ⁽³⁾	I_{AS}	10.0	A
Avalanche Energy ⁽³⁾	E_{AS}	500	mJ
Power Dissipation ⁽⁴⁾	$T_C = 25^\circ C$	313	W
	$T_C = 100^\circ C$	125	
Junction & Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$



Electrical Characteristics (@ $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
STATIC PARAMETERS						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	650		10V, I	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650\text{V}$, $V_{GS} = 0\text{V}$			10.0	μA
Gate-Body Leakage Current	I_{GSS}	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 30\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2.5	3.5	4.5	V
Static Drain-Source ON-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{V}$, $I_D = 10\text{A}$		98	110	$\text{m}\Omega$
			TO-263-3L TO-220-3L	99	110	$\text{m}\Omega$
Diode Forward Voltage	V_{SD}	$I_S = 1\text{A}$, $V_{GS} = 0\text{V}$		0.75		V
Diode Continuous Current	I_S	$T_C = 25^\circ\text{C}$		= 10V)V	10	A
DYNAMIC PARAMETERS ⁽⁵⁾						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 100\text{V}$, $f = 1\text{MHz}$		2869		pF
Output Capacitance	C_{oss}			93		pF
Effective output capacitance, energy related	$C_{o(er)}$			97		pF
Effective output capacitance, time related	$C_{o(tr)}$			410		pF
Reverse Transfer Capacitance	C_{rss}	$V_{GS} = 0\text{V}$, $V_{DS} = 100\text{V}$, $f = 1\text{MHz}$		5.4		pF
Gate Resistance	R_g			2.2		Ω
SWITCHING PARAMETERS ⁽⁵⁾						
	Q_g			72		nC
	Q_{gs}			22		nC
	Q_{gd}			33		nC
	$t_{D(on)}$			29		ns
	t_r			30		ns
	$t_{D(off)}$			77		ns
	t_f			17.4		ns
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$		152		ns
Body Diode Reverse Recovery Charge	Q_{rr}			2.5		μC
	dv/dt			15.0		V/ns
	dv/dt			50		V/ns

Parameter	Symbol	Conditions	Unit
	$R_{\theta JA}$	45	$^\circ\text{C}/\text{W}$
	$R_{\theta JC}$		$^\circ\text{C}/\text{W}$

Notes:

application board design.

Typical Electrical & Thermal Characteristics

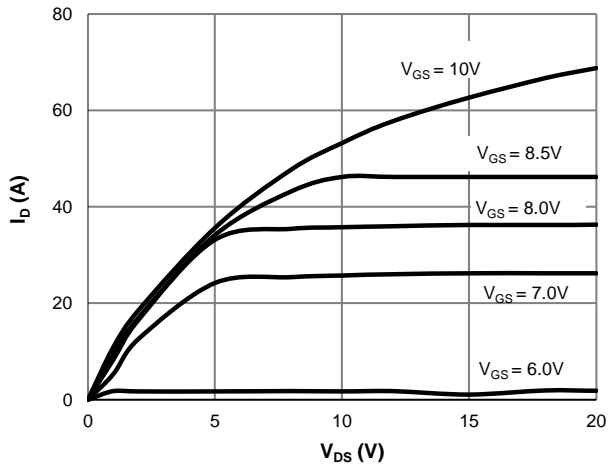


Figure 1: Saturation Characteristics

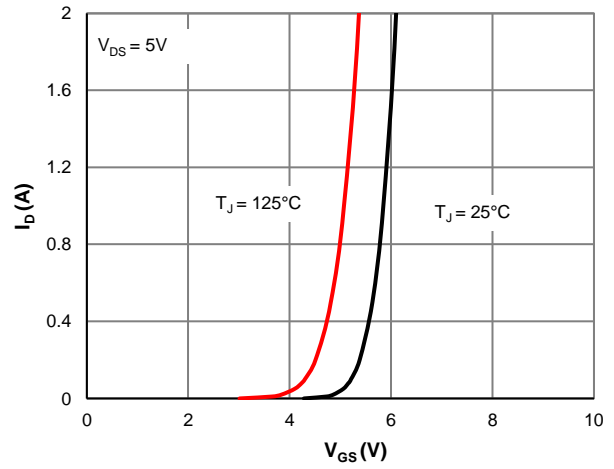


Figure 2: Transfer Characteristics

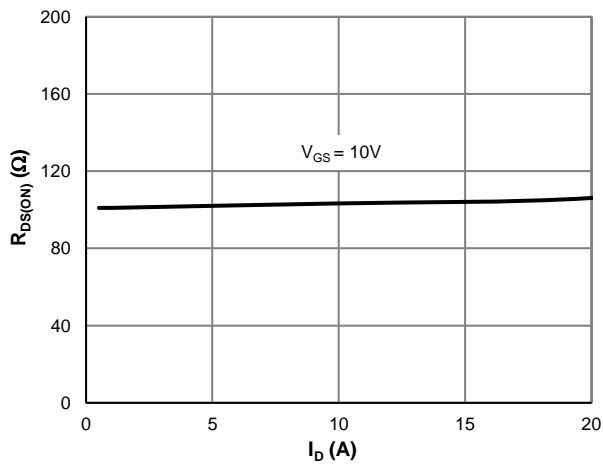


Figure 3: $R_{DS(ON)}$ vs. Drain Current

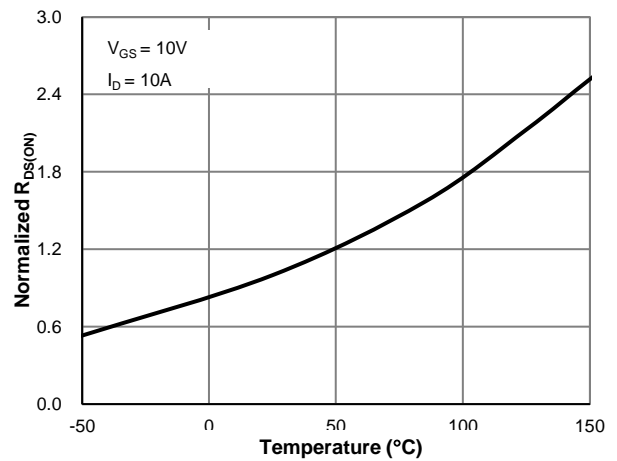


Figure 4: $R_{DS(ON)}$ vs. Junction Temperature

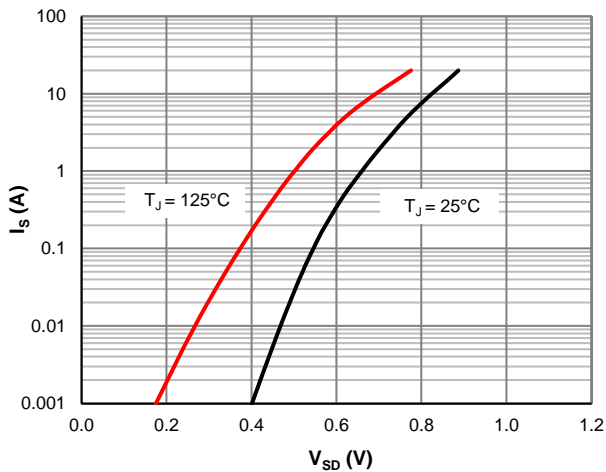


Figure 5: Body-Diode Characteristics

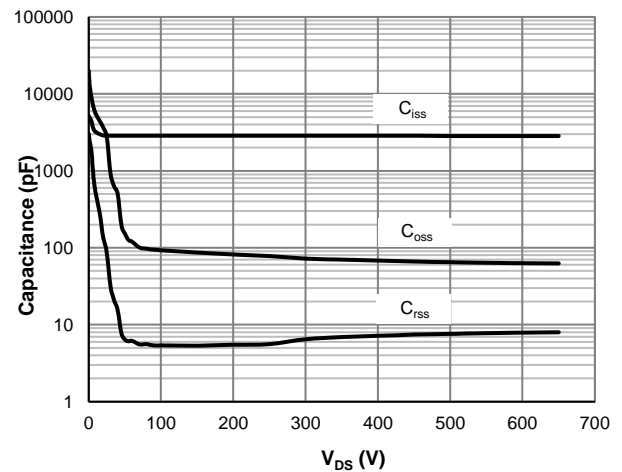


Figure 6: Capacitance Characteristics



Typical Electrical & Thermal Characteristics

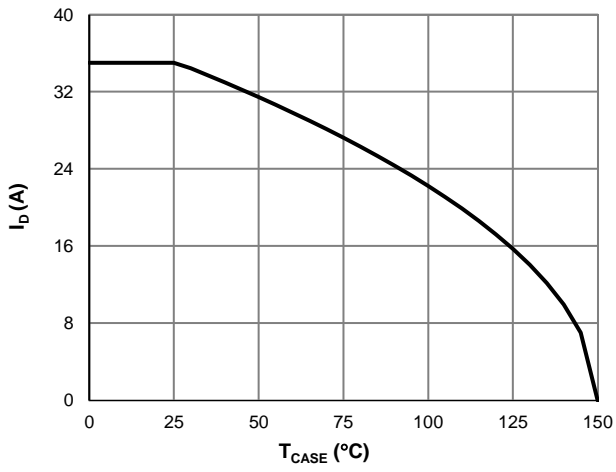


Figure 7: Current De-rating

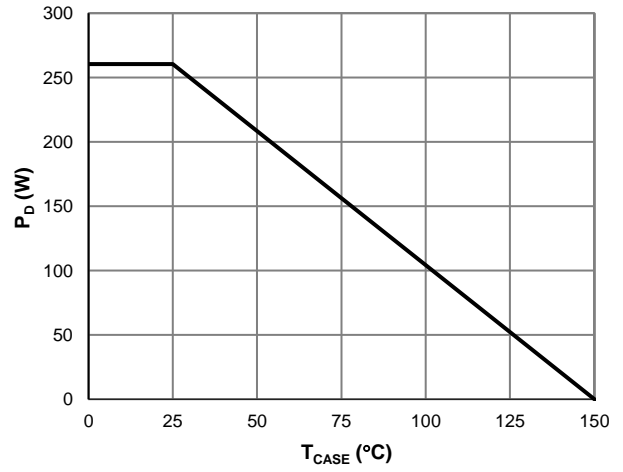


Figure 8: Power De-rating

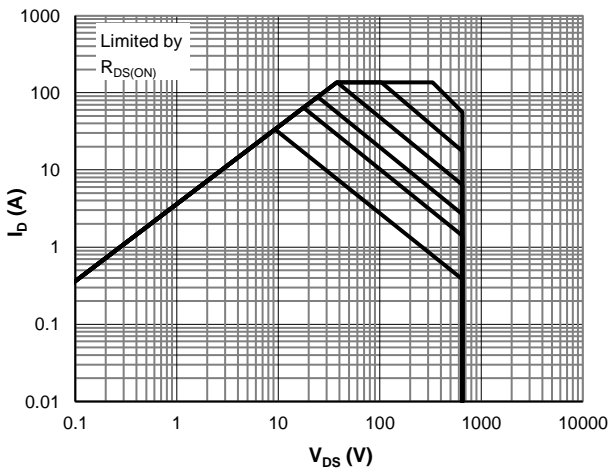
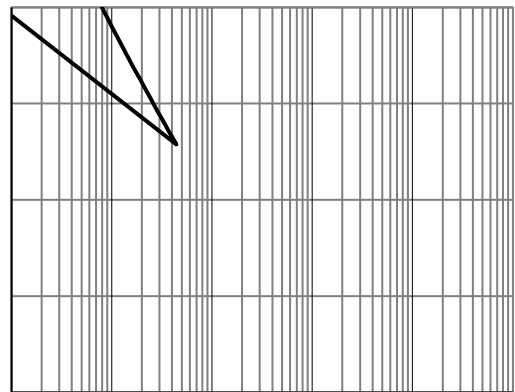
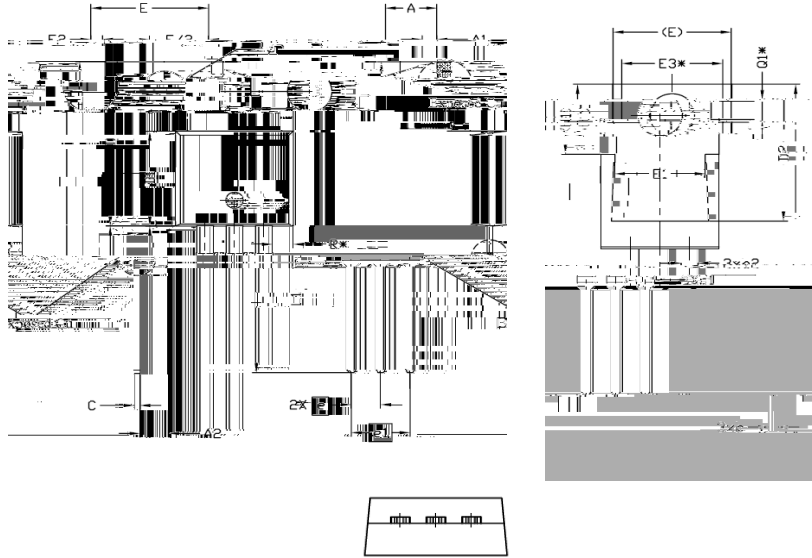


Figure 9: Maximum Safe Operating Area





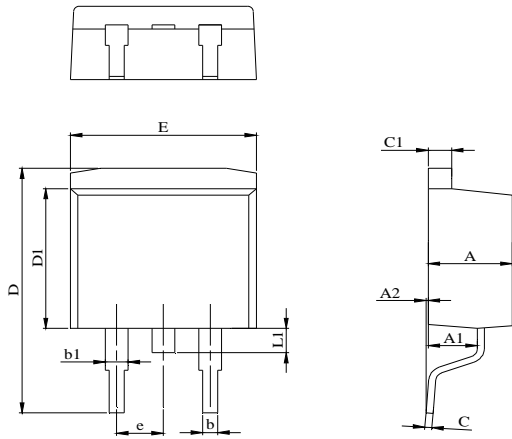
TO-220-3L Package Information



SYMBOL	DIMENSIONS (MILLIMETERS)		
	MIN.	NOM.	MAX.
A	4.24	4.44	4.64
A1	1.15	1.27	1.40
A2	2.30	2.48	2.70
b	0.70	0.80	0.90
b1	1.20	1.55	1.75
b2	1.20	1.45	1.70
c	0.40	0.50	0.60
D	14.70	15.37	16.00
D1	8.82	8.92	9.02
E	12.43	12.73	13.03
E1	12.43	12.73	13.03
E2	12.43	12.73	13.03
E3	12.43	12.73	13.03
L1	13.47	13.72	13.97
L2	3.83	3.83	4.00
L3	3.75	3.84	3.93
L4	2.60	2.80	3.00
L5	1.13	1.13	1.13
L6	1.13	1.13	1.13
L7	1.13	1.13	1.13
L8	1.13	1.13	1.13
L9	1.13	1.13	1.13
L10	1.13	1.13	1.13
L11	1.13	1.13	1.13
L12	1.13	1.13	1.13
L13	1.13	1.13	1.13
L14	1.13	1.13	1.13
L15	1.13	1.13	1.13
L16	1.13	1.13	1.13
L17	1.13	1.13	1.13
L18	1.13	1.13	1.13
L19	1.13	1.13	1.13
L20	1.13	1.13	1.13
L21	1.13	1.13	1.13
L22	1.13	1.13	1.13
L23	1.13	1.13	1.13
L24	1.13	1.13	1.13
L25	1.13	1.13	1.13
L26	1.13	1.13	1.13
L27	1.13	1.13	1.13
L28	1.13	1.13	1.13
L29	1.13	1.13	1.13
L30	1.13	1.13	1.13
L31	1.13	1.13	1.13
L32	1.13	1.13	1.13
L33	1.13	1.13	1.13
L34	1.13	1.13	1.13
L35	1.13	1.13	1.13
L36	1.13	1.13	1.13
L37	1.13	1.13	1.13
L38	1.13	1.13	1.13
L39	1.13	1.13	1.13
L40	1.13	1.13	1.13
L41	1.13	1.13	1.13
L42	1.13	1.13	1.13
L43	1.13	1.13	1.13
L44	1.13	1.13	1.13
L45	1.13	1.13	1.13
L46	1.13	1.13	1.13
L47	1.13	1.13	1.13
L48	1.13	1.13	1.13
L49	1.13	1.13	1.13
L50	1.13	1.13	1.13
L51	1.13	1.13	1.13
L52	1.13	1.13	1.13
L53	1.13	1.13	1.13
L54	1.13	1.13	1.13
L55	1.13	1.13	1.13
L56	1.13	1.13	1.13
L57	1.13	1.13	1.13
L58	1.13	1.13	1.13
L59	1.13	1.13	1.13
L60	1.13	1.13	1.13
L61	1.13	1.13	1.13
L62	1.13	1.13	1.13
L63	1.13	1.13	1.13
L64	1.13	1.13	1.13
L65	1.13	1.13	1.13
L66	1.13	1.13	1.13
L67	1.13	1.13	1.13
L68	1.13	1.13	1.13
L69	1.13	1.13	1.13
L70	1.13	1.13	1.13
L71	1.13	1.13	1.13
L72	1.13	1.13	1.13
L73	1.13	1.13	1.13
L74	1.13	1.13	1.13
L75	1.13	1.13	1.13
L76	1.13	1.13	1.13
L77	1.13	1.13	1.13
L78	1.13	1.13	1.13
L79	1.13	1.13	1.13
L80	1.13	1.13	1.13
L81	1.13	1.13	1.13
L82	1.13	1.13	1.13
L83	1.13	1.13	1.13
L84	1.13	1.13	1.13
L85	1.13	1.13	1.13
L86	1.13	1.13	1.13
L87	1.13	1.13	1.13
L88	1.13	1.13	1.13
L89	1.13	1.13	1.13
L90	1.13	1.13	1.13
L91	1.13	1.13	1.13
L92	1.13	1.13	1.13
L93	1.13	1.13	1.13
L94	1.13	1.13	1.13
L95	1.13	1.13	1.13
L96	1.13	1.13	1.13
L97	1.13	1.13	1.13
L98	1.13	1.13	1.13
L99	1.13	1.13	1.13
L100	1.13	1.13	1.13

TO-263-3L Package Information

Package Outline



Recommend Soldering Footprint

